We Claim:

1. A test configuration, comprising:

a support material;

a semiconductor chip disposed on said support material, said semiconductor chip having a self-test unit generating test information for functionally checking said semiconductor chip; and

an energy source for providing an electrical energy supply from energy that is fed in contactlessly, said energy source disposed on said support material and connected to said semiconductor chip for providing the electrical energy supply to said semiconductor chip.

2. The test configuration according to claim 1, wherein said energy source has at least one solar cell for generating an operating current for said semiconductor chip by optical radiation that is fed in contactlessly.

3. The test configuration according to claim 2, wherein said support material is a semiconductor wafer, and said semiconductor chip is one of a plurality of semiconductor chips disposed on said semiconductor wafer, said

semiconductor wafer has a scribe line for separating said semiconductor chips from one another, and said solar cell is disposed in said scribe line.

4. The test configuration according to claim 2, wherein said solar cell is disposed on said semiconductor chip.

5. The test configuration according to claim 2, wherein said support material is a semiconductor wafer, and said solar cell is disposed areally on a surface of said semiconductor wafer.

6. The test configuration according to claim 2, wherein said solar cell is disposed on a surface of said support material which is remote from said semiconductor chip, said support material having an electrically conductive plated-through hole formed therein disposed between said solar cell and said semiconductor chip, at a boundary between said plated-through hole and said support material, said support material has a pn junction disposed along said plated-through hole for preventing a current flow between said plated-through hole and a remainder of said support material.

7. The test configuration according to claim 4, including a radiation-absorbing layer disposed between said solar cell and said semiconductor chip.

8. The test configuration according to claim 1, wherein said semiconductor chip has a functional unit for a contactless transmission of data containing information about a test result.

9. The test configuration according to claim 8, including a receiver, and said functional unit generates optical radiation pulses in accordance with the data to be transmitted, which can be received by said receiver disposed separate from said semiconductor chip.

10. The test configuration according to claim 8, including a receiver disposed separate from said semiconductor chip, said functional unit has an output terminal through which the data to be transmitted can be transmitted by capacitive coupling to said receiver.

11. The test configuration according to claim 10, wherein said semiconductor chip has a material layer connected to said output terminal of said functional unit, at which a potential, which can be controlled by said functional unit, is present in accordance with the data to be transmitted, said material layer effects an optical refraction of optical radiation and the optical refraction can be controlled by the potential, said material layer can be irradiated with the optical

radiation and the optical radiation refracted by said material layer can be received by said receiver.

12. The test configuration according to claim 8, wherein said semiconductor chip has a detector selected from the group consisting of voltage detectors and current detectors, said detector is connected to said energy source and to said functional unit for initiating a data transmission by said functional unit on account of a detected characteristic voltage sequence or current sequence.

13. The test configuration according to claim 1, wherein said semiconductor chip has a terminal and a nonvolatile memory unit for storing data containing information about a test result, said nonvolatile memory unit is connected to said terminal through which the data of said nonvolatile memory unit can be tapped off to a point outside said semiconductor chip.

14. The test configuration according to claim 1, wherein said semiconductor chip is one of a plurality of semiconductor chips to be tested, and one of said plurality of semiconductor chips to be tested is decoupled from respective others of said plurality of semiconductor chips with regard to said energy supply during a functional test.

15. The test configuration according to claim 1, wherein said semiconductor chip is one of a plurality of semiconductor chips to be tested and all connected to said energy source being a common energy source, each of said semiconductor chips have a current limiter circuit for electrically isolating a respective semiconductor chip from said common energy source in an event of a limit value of an operating current being exceeded.

16. The test configuration according to claim 1, wherein said semiconductor chip has a detector selected from the group consisting of voltage detectors and current detectors, said detector connected to said energy source and to said self-test unit for initiating a functional test on account of a detected characteristic voltage sequence or current sequence.

17. The test configuration according to claim 1, wherein said semiconductor chip has an integrated memory containing memory cells which can be subjected to a functional test, and said self-test unit generates test information and carries out a functional test of said memory cells.

18. The test configuration according to claim 17, wherein said integrated memory has normal memory cells and redundant memory cells for replacing said normal memory cells, said self-test unit is configured for checking a functionality of

said normal memory cells, for analyzing which of said normal memory cells are to be replaced by which of said redundant memory cells, and for activating said redundant memory cells in accordance with a result of the analysis.

19. The test configuration according to claim 18, wherein said integrated memory has electrically programmable memory units for activating said redundant memory cells, in which a repair result determined by said self-test unit can be programmed.